

Additional Services

Take advantage of BittWare's range of design, integration, and support options



Customization

[Additional specification options](#) or [accessory boards](#) to meet your exact needs.



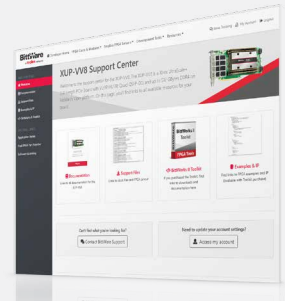
Server Integration

Available pre-integrated in our [TeraBox servers](#) in a range of configurations.



Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

FPGA	<ul style="list-style-type: none"> Intel Stratix 10 MX <ul style="list-style-type: none"> MX2100 in an F2597 package 16GBytes on-chip High Bandwidth Memory (HBM2) DRAM, 410 GB/s (speed grade 2) Core speed grade -2: I/O speed grade -2 Contact BittWare for other Stratix 10 MX options
On-board Flash	<ul style="list-style-type: none"> 2Gbit Flash memory for booting FPGA
External memory	<ul style="list-style-type: none"> 2x 288-pin DIMM slots each fitted with 16GB modules by default, i.e., 32GB total on board (options up to 256GB total) Contact BittWare for QDR-II+ & Intel Optane (3D-Xpoint) DIMM options
Host interface	<ul style="list-style-type: none"> x16 Gen3 interface direct to FPGA, connected to PCIe hard IP
QSFP cages	<ul style="list-style-type: none"> 4 QSFP28 cages on front panel connected directly to FPGA via 16 transceivers User programmable low jitter clocking supporting 10/25/40/100GbE Each QSFP28 can be independently clocked Jitter cleaner for network recovered clocking 2 QSFP28s have available 100GbE MAC hard IP
OCuLink	<ul style="list-style-type: none"> 2x edge connectors (A, B) @ 12.5G per lane (default); each supports PCIe Gen 3 x8 hard IP, GPIO, and PCIe master and optional input clocking 2x inner connectors (C, D) @ 25G per lane (optional); 1x 100GbE MAC hard IP per OCuLink
Board Management Controller	<ul style="list-style-type: none"> Voltage, current, temperature monitoring Power sequencing and reset Field upgrades FPGA configuration and control Clock configuration Low bandwidth BMC-FPGA comms with SPI link USB 2.0 PLDM support Voltage overrides

Cooling	<ul style="list-style-type: none"> Standard: dual-slot active heatsink (with fan) Optional: dual-slot passive heatsink Optional: dual-slot liquid cooling
Electrical	<ul style="list-style-type: none"> On-board power derived from PCIe slot 12V and two AUX connectors (one 8-pin, one 6-pin) Power dissipation is application dependent Typical max power consumption 225W
Environmental	<ul style="list-style-type: none"> Operating temperature: 5°C to 35°C
Quality	<ul style="list-style-type: none"> Manufactured to IPC-A-610 Class 2 RoHS compliant CE, FCC & ICES approvals
Form factor	<ul style="list-style-type: none"> Standard-height PCIe dual-slot board 4.376 x 10.5 inches (111 x 266.7 mm)

Development Tools

FPGA development	BIST - Built-In Self-Test for CentOS 7 provided with source code (pinout, gateway, PCIe driver and host test application)
Application development	Supported design flows - Intel FPGA OpenCL SDK, Intel High-Level Synthesis (C/C++) and Quartus Prime Pro (HDL, Verilog, VHDL, etc.)

Deliverables

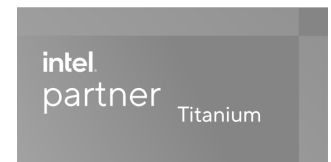
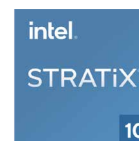
- 520N-MX FPGA board
- USB cable (front panel access)
- Built-In Self-Test (BIST)
- OpenCL HPC Board Support Package (BSP)
- 1-year access to online Developer Site
- 1-year hardware warranty

To learn more, visit www.BittWare.com

Rev 2021.11.23 | November 2021

© BittWare 2021

Stratix 10 is a registered trademark of Intel Corp. All other products are the trademarks or registered trademarks of their respective holders.



BittWare
a **molex** company